REMARKS

Claims 1-39 remain pending in the application. Claims 1, 5, 9, 15, 16, 26, 30, 32 and 34 have been amended. No new matter has been added. Applicant respectfully requests reconsideration in view of the foregoing amendments and these remarks.

I. Interview

Applicant wishes to thank the Examiner for an in person interview that was conducted with Applicant's representative and the Examiner on July 10, 2006. During the interview the Lin reference was discussed with reference to claim 1. No agreement was reached.

II. Allowable claims

Applicant wishes to thank the Examiner for indicating that claims 5-7, 9-12, 16-21, 30-32 and 34-37 were merely objected to as being dependent upon a rejected base claim, but would otherwise be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicant has amended these claims to include the underlying limitations and believes that these claims as such are in condition for allowance.

III. 35 USC 102 Rejection

Claims 1-4, 8, 13-15, 22-29, 33 and 38-39 stand rejected under 35 USC 102(e) as being anticipated by Lin, published United States Patent Application 2002/0157031 (hereinafter referred to as "Lin"). Applicant respectfully traverses the rejection.

a. Claim 1 and its dependent claims

Claim 1 is directed to a sampling device that includes a first delay circuit and a second delay circuit in a parallel configuration and a control circuitry. The first delay circuit and the second delay circuit are responsive to a clock signal and each of the first and second delay circuits are independent and provide separate output signals to a sampling circuit. The control circuitry is responsive to an output of the first delay circuit and the clock signal and adjusts a delay amount of the first delay circuit based on a difference between the output of the first delay circuit and the clock signal. The control circuitry is further responsive to an output of the second delay circuit and adjusts a delay amount of the second delay circuit based on a difference between the output of the second delay circuit and the clock signal.

The Examiner has suggested that Lin teaches all of the limitations set forth in claim 1. Applicant respectfully disagrees. Applicant respectfully submits that Lin does not teach parallel first and second delay circuits that are independent and provide separate output signals to a sampling circuit.

Lin shows circuitry including a master delay locked loop (DLL) and a slave DLL. The master DLL includes a delay line 160 and the slave DLL includes delay lines 140 and 142. However, Lin's delay lines are not the same as Applicant's claimed parallel first and second delay circuits that are independent and provide separate output signals to a sampling circuit. As an initial matter, Applicant respectfully asserts that Lin's delay lines are not configured in a parallel configuration. In fact, delay line 160 is configured in series with delay line 140 when the delay line is active in Lin's circuit. More specifically, the slave DLL 114 is active providing a clock signal that eventually results in data being latched by latch 130 only when multiplexor (mux) 116 is toggled by the select signal 156. When active, the slave DLL 114 provides an input to the master DLL 112 through mux 116, resulting in the delay line 140 being effectively placed in series with the delay line 160. Accordingly, Applicant respectfully asserts that Lin's configuration is not parallel as recited in claim 1. In fact, Lin's slave delay line is in series with the master delay line when providing a sampling clock to the latch 130.

As an additional matter, Applicant respectfully asserts that Lin's delay lines are not independent and do not provide separate output signals to a sampling circuit. As discussed above, the output of the slave DLL 114 is provided as an input to the master DLL 112. Accordingly, the output of the slave DLL 114 is not separate from the output of the master DLL 112, the former providing an input to the later. Only Lin's master DLL 112 provides an output to Lin's sampling circuitry (latch 130). Applicant respectfully asserts that, for at least this additional reason, Lin does not teach or suggest Applicant's claimed sampling device as recited in claim 1.

Claims 2-4, 8, 13 and 14 depend from claim 1 and are allowable for at least the same reasons set forth above with respect to claim 1.

b. Claim 15 and its dependent claims

Claim 15 is directed to a method of sampling data that includes receiving a clock signal synchronized with a data signal, generating a first sampling signal based on the clock signal, the first sampling signal delayed by a first delay with respect to the clock signal, generating a second separate sampling signal based on the clock signal where the second separate sampling signal is delayed by a second delay with respect to the clock signal that is different than and independent from the first delay. The method includes sampling the data with the first and second sampling signals.

As discussed above, the master and slave DLLs of Lin are cascaded and result in a delay that is applied to a clock signal that is always affected by the delay applied by the master DLL. That is, Lin's master and slave DLL configuration does not provide Applicant's claimed second delay that is independent from the first delay. Lin's delay in the clock signal that is provided to the latch 130 is always influenced by the delay line 160. Lin's delay line 160 is always in the path to the latch 130 irrespective of the configuration of the slave DLL and the mux 116. Applicant respectfully asserts that Lin does not teach or suggest generating a second sampling signal that is delayed by a second delay that is independent from a first delay.

Claims 22-25 depend from claim 15 and are allowable for at least the same reasons set forth above with respect to claim 15.

c. Claim 26 and its dependent claims

Claim 26 is directed to a sampling circuit that includes a first delaying means and a second delaying means in a parallel configuration. The first delaying means and the second delaying means are for receiving a clock signal and for generating one or more delayed signals based on the clock signal. Each of the first and second delaying means is independent and provides separate output signals to a data sampling means.

Claim 26 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 27-29, 33, 38 and 39 depend from claim 26 and are allowable for at least the same reasons set forth above with respect to claim 26.

Applicant : Eitan Rosen
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Applicant respectfully requests a three-month extension of time up to and including September 9, 2006. Enclosed is a credit card authorization for excess claim fees and for the Petition for Extension of Time fee for responding to the outstanding action up and until September 8, 2006. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 9-8-06

42,596

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